AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A reference voltage generating circuit comprising an active resistance part having a plurality of MOS transistors connected between an external voltage and a ground voltage,

each of the plurality of MOS transistors having a gate electrode which receives an enable voltage at a potential higher than a voltage potential between drain and source electrodes of each of the plurality of MOS transistors to operate in a linear current-voltage region~~, wherein gate electrodes of each the plurality of MOS transistors are connected to a common node for receiving the enable voltage~~,

a current mirror circuit comprising first and second PMOS transistors, a source of each of the first and second PMOS transistors receiving the external voltage, wherein the current mirror circuit is electrically connected to the active resistance part, and

a voltage supply circuit comprising a third PMOS transistor and a plurality of NMOS transistors, wherein the voltage supply circuit supplies the enable voltage to the plurality of MOS transistors, wherein the enable voltage is determined by the NMOS transistors,

wherein a gate of the third PMOS transistor is connected to a drain of the first PMOS transistor, a source of the third PMOS transistor receives the external voltage and is connected to a back gate of the third PMOS transistor, and a drain of the third PMOS

transistor is connected to a drain and a gate of a first NMOS transistor of the plurality of NMOS transistors.

2. (Previously Canceled)

3. (Previously Amended) The circuit as claimed in claim 1, wherein the plurality of MOS transistors are connected in series between the external voltage and the ground voltage.

4. (Previously Canceled)

5. (Previously Canceled)

6. (Currently Amended) A reference voltage generating circuit comprising:

a current mirror circuit having first and second current paths formed between a first power source terminal and a second power source terminal, the current mirror circuit being operated in response to a voltage level of the second current path;

a reference voltage output node for providing a reference voltage, the reference voltage output node being located on the second current path;

an active resistance device formed on the first current path to be operated in a linear region of a current-voltage characteristic curve of the active resistance device; and

a voltage supply circuit for supplying the active resistance device with an enable voltage to control the active resistance device to be operated in the linear region, wherein the voltage supply circuit includes a PMOS transistor and a plurality of NMOS transistors, wherein the enable voltage is determined by the NMOS transistors and obtained at a node between the PMOS transistor and the plurality of NMOS transistors,

wherein a gate of the PMOS transistor is connected to a drain of a first PMOS transistor formed on the first current path, a source of the PMOS transistor receives an

externally applied voltage and is connected to a back gate of the PMOS transistor, and a drain of the PMOS transistor is connected to a drain and a gate of a first NMOS transistor of the plurality of NMOS transistors.

7. (Previously Canceled)

8. (Currently Amended) The circuit as claimed in claim ~~7~~ 6, wherein the active resistance device is a single MOS transistor having a gate electrode for receiving the enable voltage from the voltage supply circuit.

9. (Previously Amended) The circuit as claimed in claim 8, wherein the enable voltage is higher than a voltage between drain and source electrodes of the MOS transistor.

10. (Currently Amended) The circuit as claimed in claim ~~7~~ 6, wherein the active resistance device includes a plurality of MOS transistors arranged in series on the first current path, gate electrodes of the plurality of MOS transistors receive the enable voltage from the voltage supply circuit.

11. (Previously Amended) The circuit as claimed in claim 10, wherein the enable voltage is higher than a sum of voltages, wherein each voltage is obtained between drain and source electrodes of a corresponding one of the plurality of MOS transistors.

12. (Previously Canceled)

13. (Currently Amended) The circuit as claimed in claim 6, wherein the first power source terminal receives the externally applied voltage and the second power source terminal is connected to a ground voltage.

14. (Original) The circuit as claimed in claim 6, further including a current control unit for controlling current flowing in the first and second current paths by employing MOS transistors formed on the first and second current paths, respectively.

15. (Currently Amended) The circuit as claimed in claim 6, wherein the current mirror circuit includes ~~a~~ the first ~~pair of~~ PMOS transistor~~s~~ formed on the first ~~and second~~ current path~~s, respectively~~ and a second PMOS transistor formed on the second current path.

16. (Currently Amended) A reference voltage generating circuit comprising:

a current mirror circuit having first and second MOS transistors, sources of the first and second MOS transistors receiving an externally applied voltage, a gate of the first MOS transistor being connected to a gate of the second MOS transistor and to a drain of the first MOS transistor;

a current control circuit having third and fourth MOS transistors, a drain of the third MOS transistor being connected to the drain of the first MOS transistor, a drain of the fourth MOS transistor being connected to a gate of the third MOS transistor and a drain of the second MOS transistor, a source of the fourth MOS transistor being connected to a ground, and a reference voltage being provided on a node between the drain of the second MOS transistor and the drain of the fourth MOS transistor;

an active resistance circuit having a fifth MOS transistor, a drain of the fifth MOS transistor being connected to a gate of the fourth MOS transistor and a source of the third MOS transistor, a source of the fifth MOS transistor being connected to the ground, and a gate of the fifth MOS transistor receives a control voltage higher than a voltage between

the drain and source of the fifth MOS transistor so that the fifth MOS transistor is operated in a linear region; and

a voltage supply circuit having a PMOS transistor and a set of NMOS transistors, wherein the voltage supply circuit supplies ~~the~~ an enable voltage to the ~~plurality of~~ fifth MOS transistors ~~of the active resistance circuit~~, wherein the enable voltage is determined by the set of NMOS transistors,

wherein a gate of the PMOS transistor is connected to the drain of the first MOS transistor, a source of the PMOS transistor receives the externally applied voltage and is connected to a back gate of the PMOS transistor, a drain of the PMOS transistor is connected to a drain and gate of a first NMOS transistor of the set of NMOS transistors which are connected in series between the PMOS transistor and the ground, and the control voltage is provided from a node between the PMOS transistor and the first NMOS transistor of the set of NMOS transistors to the gate of the fifth MOS transistor.

17. (Canceled)

18. (Currently Amended) The circuit as claimed in claim ~~17~~ 16, wherein the active resistance circuit further includes sixth through n_{th} MOS transistors, the fifth through n_{th} MOS transistors being connected in series between the current control circuit and the ground, and gates of the respective fifth through n_{th} MOS transistors receiving the control ~~signal~~ voltage from the voltage supply circuit.

19. (New) The circuit as claimed in claim 1, wherein gate electrodes of each of the plurality of MOS transistors of the active resistance part are connected to a common node for receiving the enable voltage.